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6	CPU-Power
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11	PCH-SATA/HOST/GPIO/DDI/VGA
12	PCH-SMB/LPC/AUDIO/RTC
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14	PCH-GND
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MS-7829

Version : 0A

CPU :

Intel Haswell Processor

System Chipset :

Intel Lynx Point Chipset

On Board Chipset :

VRM 12.5 --ISL95816HRZ 4 Phase

Gigabit Intel Clarkville-V I217

HDA Codec -- Realtek ALC662-VD

Super I/O -- NCT5533D

SPI Flash 32Mb


Main Memory :

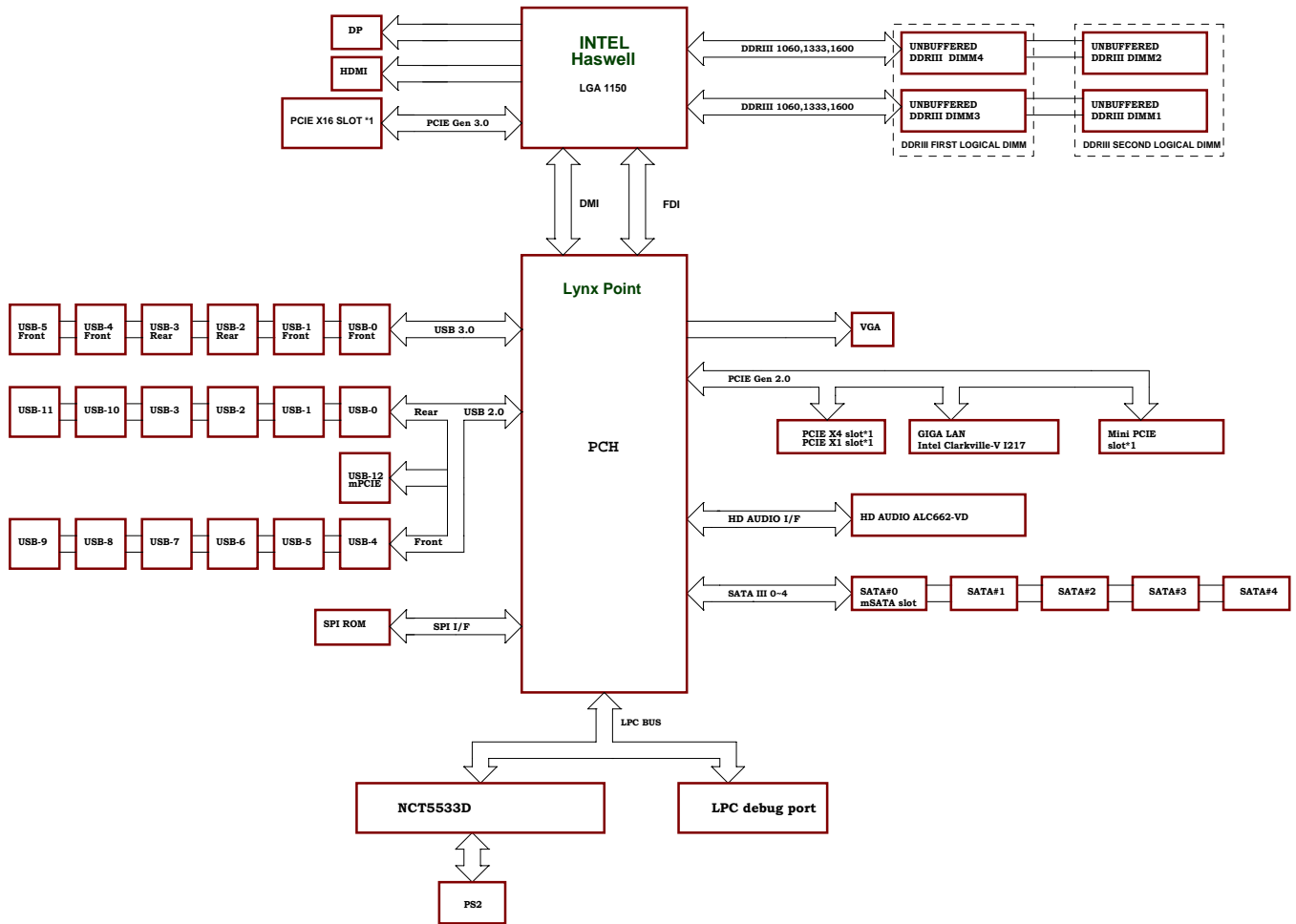
2 Channel DDR III * 4 (Max 32GB)

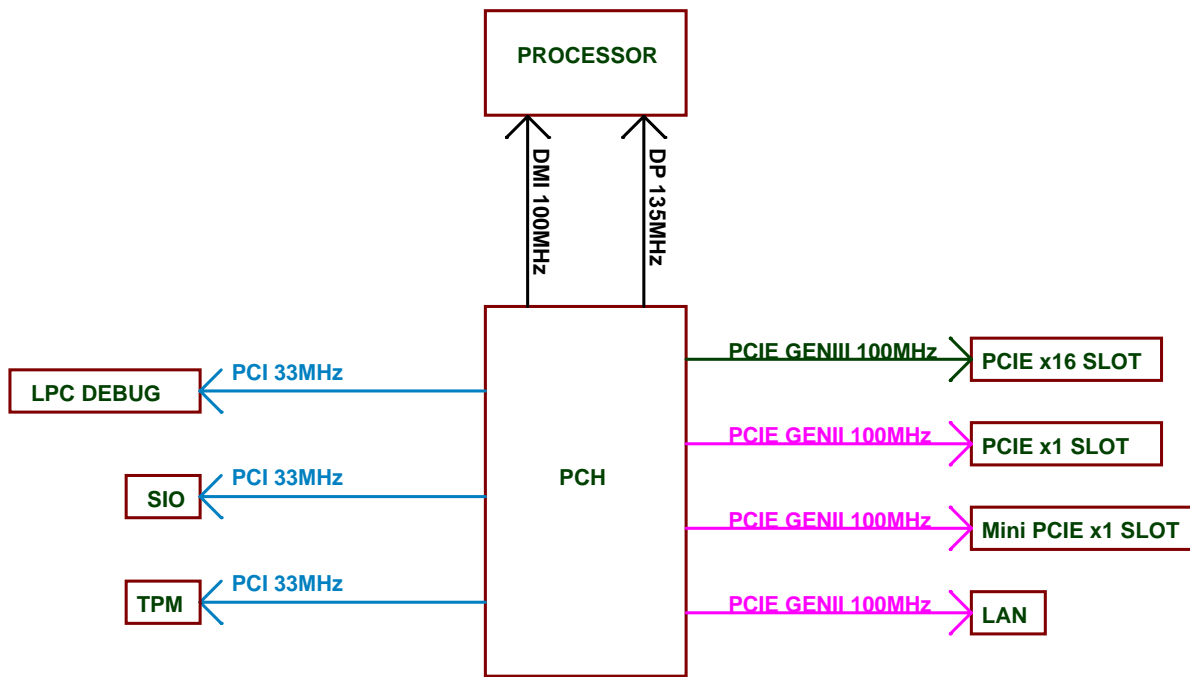
Expansion Slot :

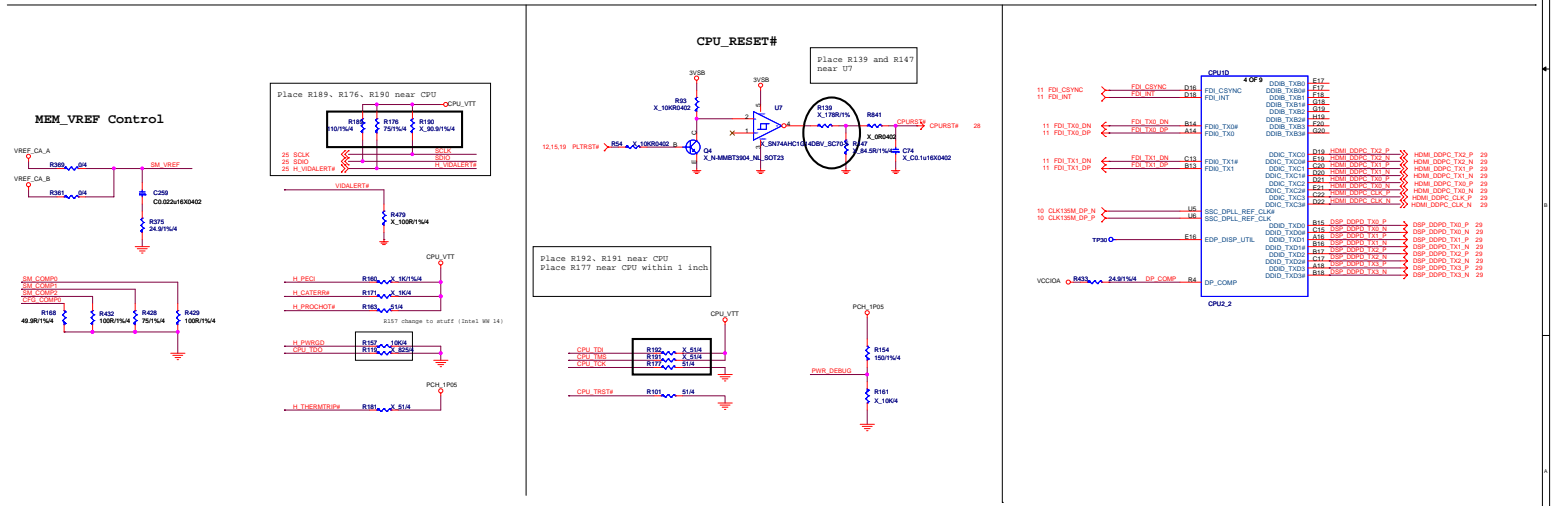
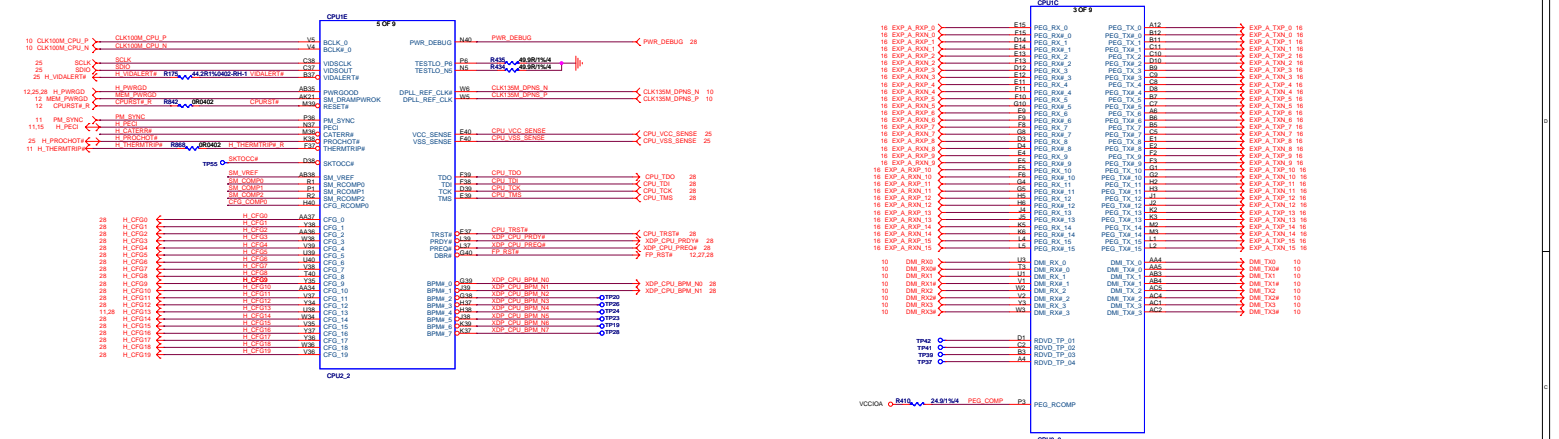
PCI Express x16 Slot * 1

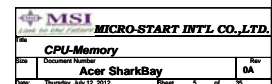
Mini PCIE/Mini SATA Slot * 1

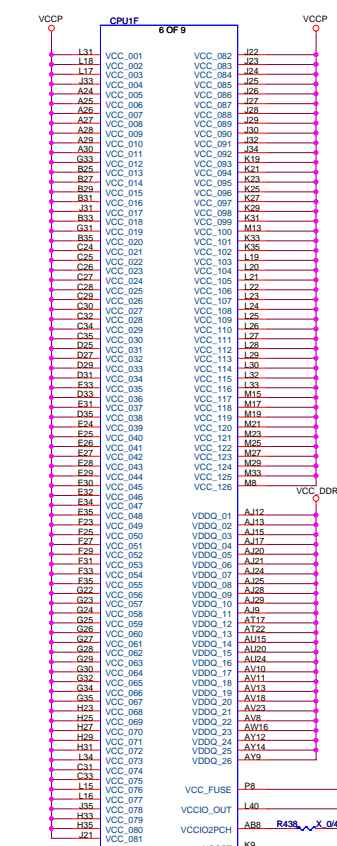
 MICRO-START INTL CO.,LTD.		
Link to the Factory		
Cover Sheet		
Size	Document Number	Rev
	Acer SharkBay	0A
Date	Friday, July 06, 2012	Sheet 1 of 36



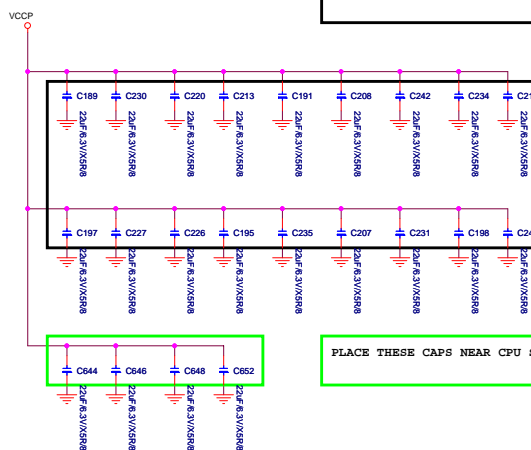




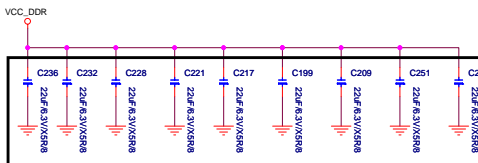


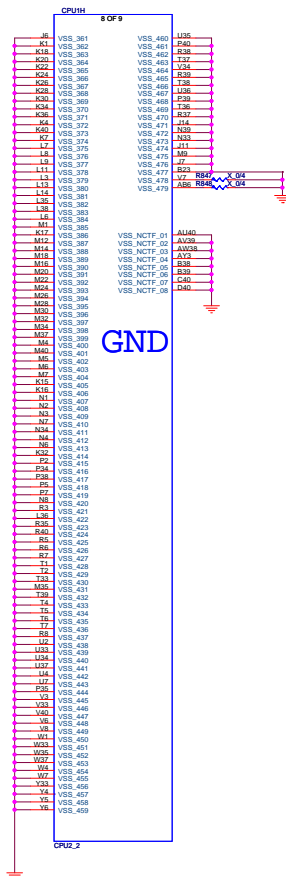
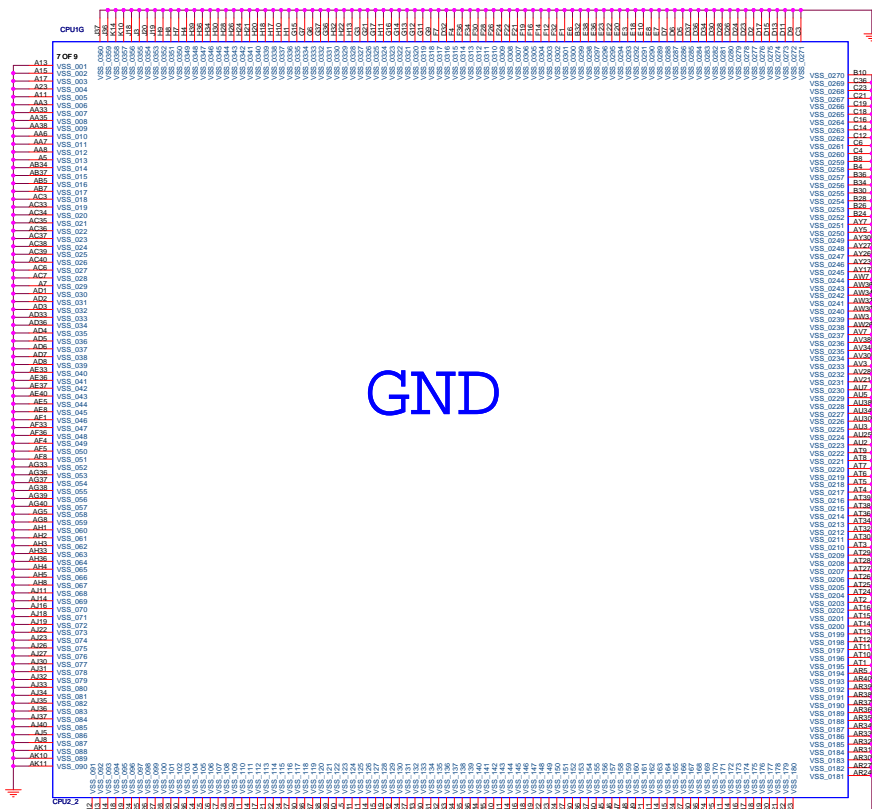


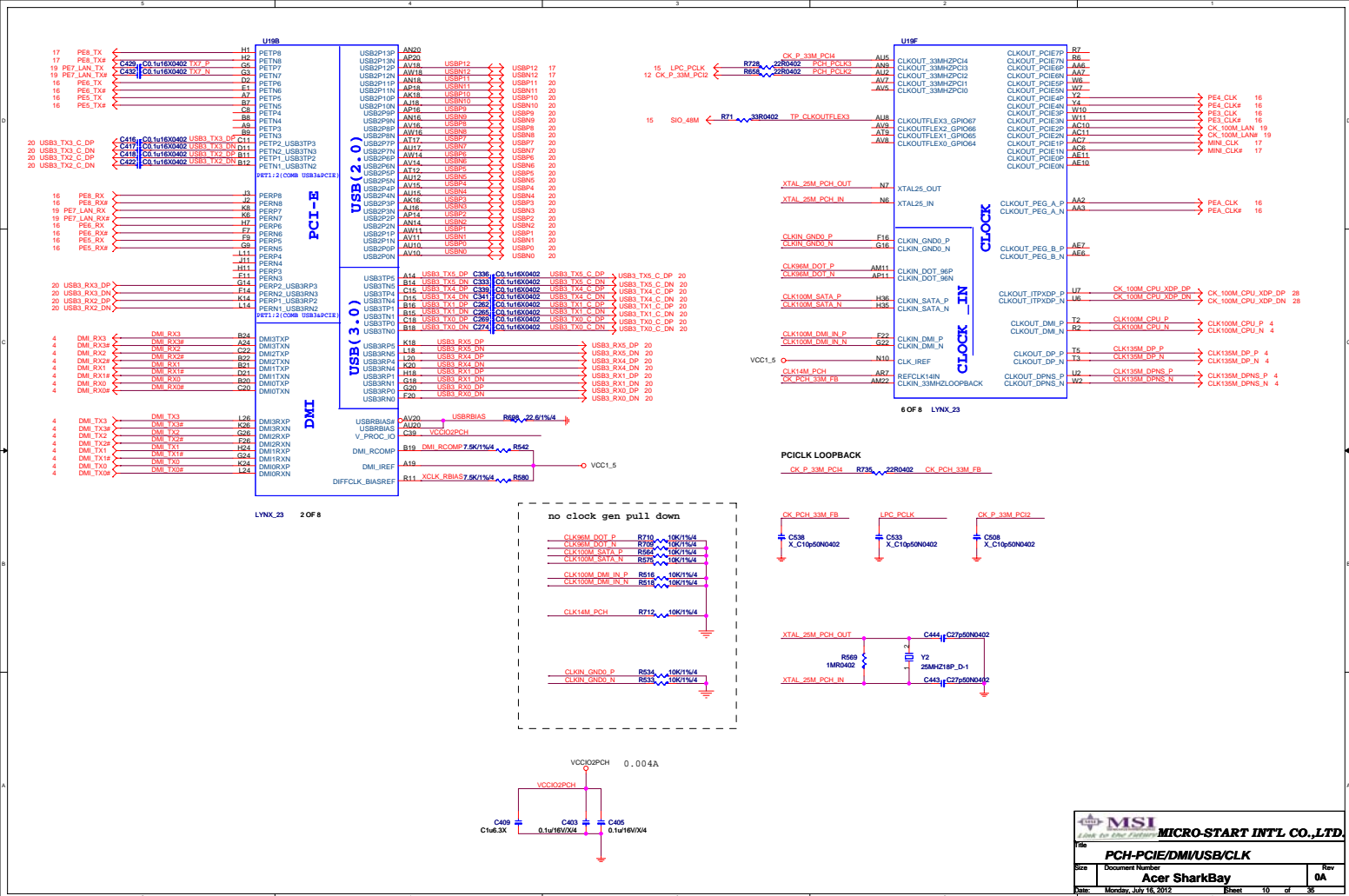
VCCP-Decoupling

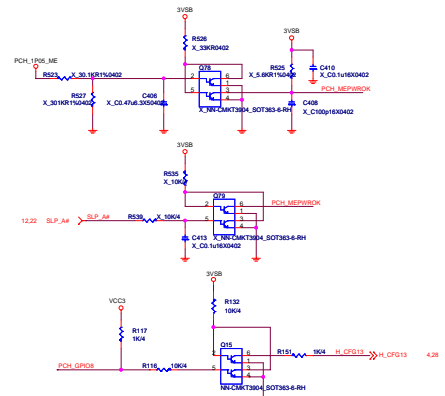
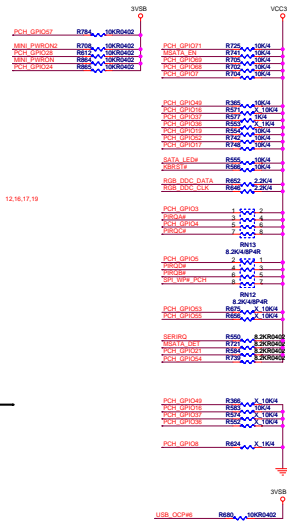
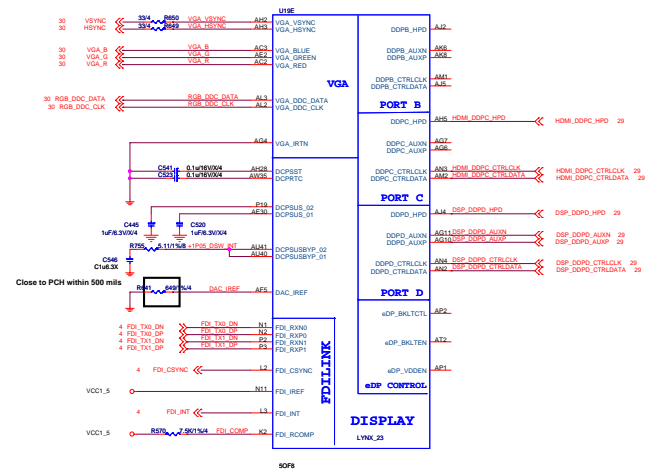
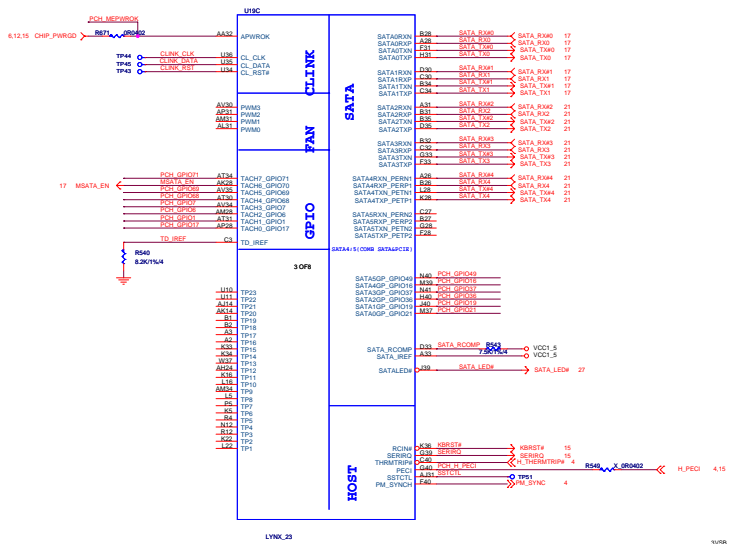


VCC_DDR-Decoupling







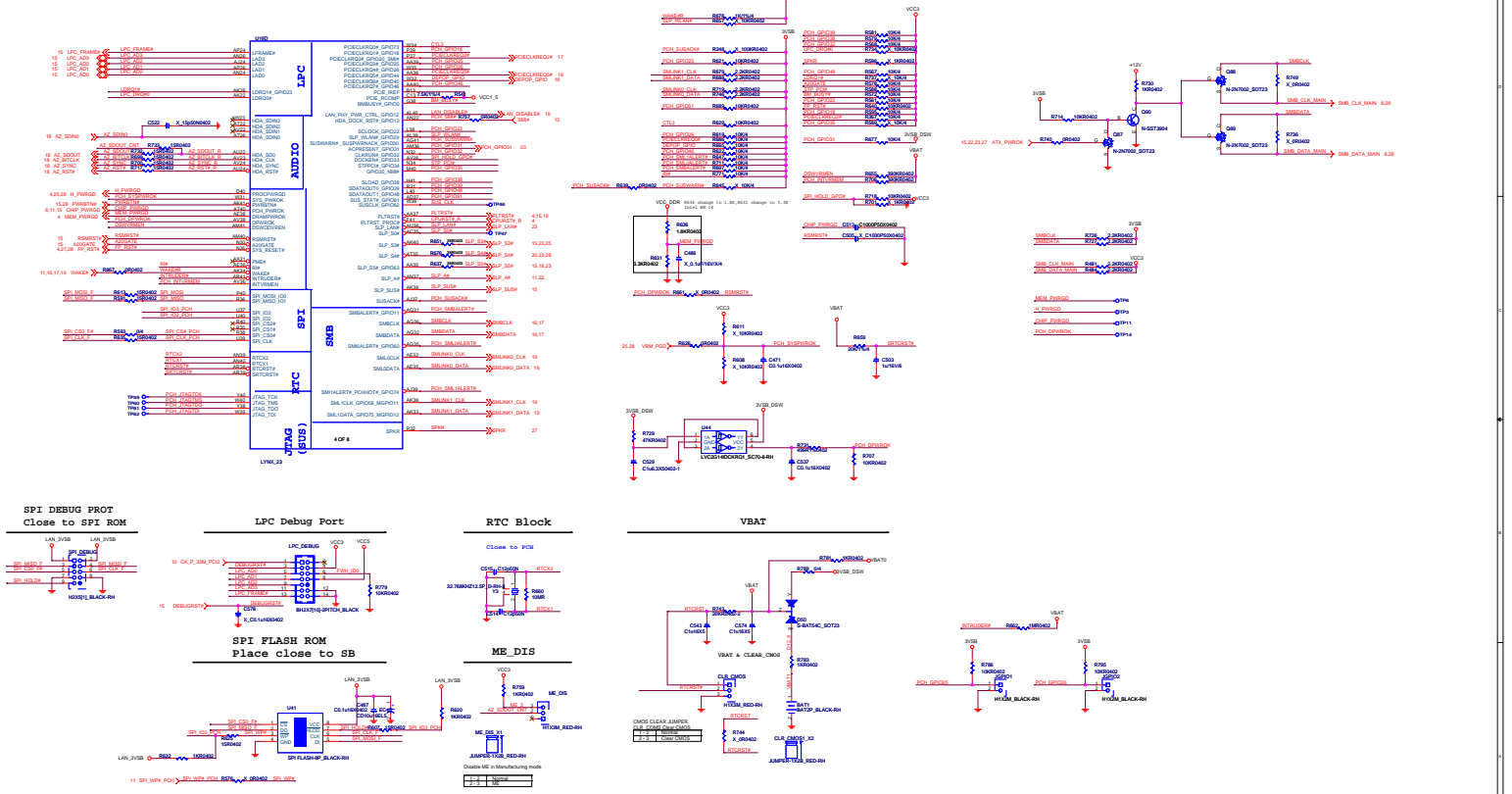


BIOS STARAPPS

BIOS STARAPPS	GPI01	GPI06
0A	1	1
NA	0	0

BIOS Device Select

BIOS Device Select	GPI051	GPI019
LPC	0	0
SPI	1	1



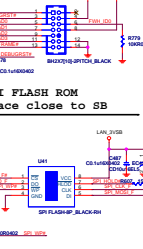
SPI DEBUG PROT

Close to SPI ROM



LFC Debug Port

Close to SPI ROM



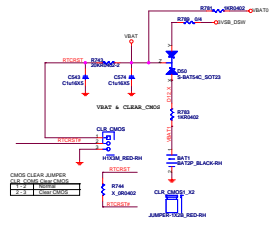
RTC Block

Close to SPI ROM

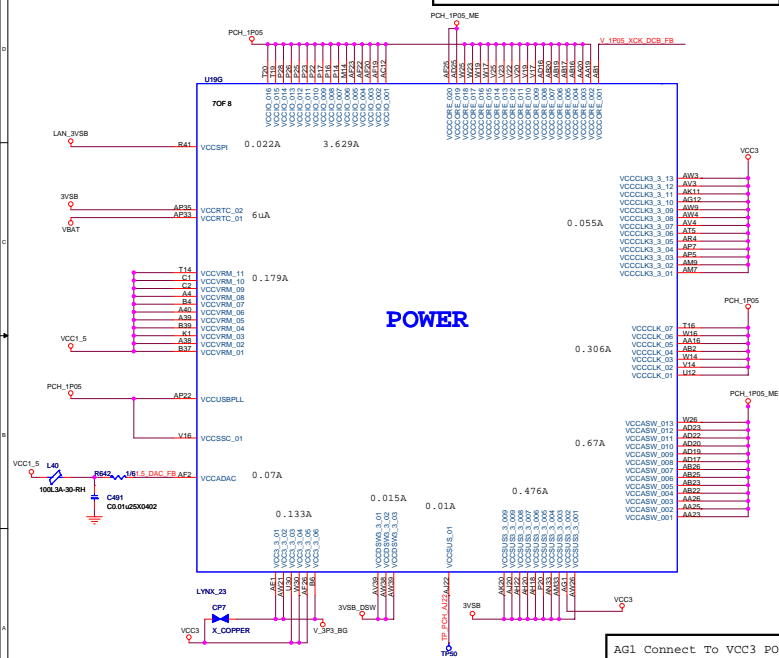


VBAT

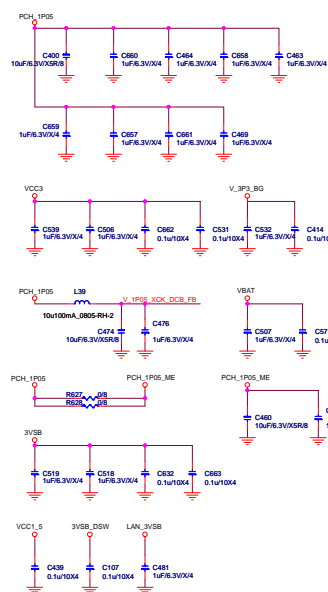
Close to SPI ROM



AF25, AD25 Connect To ASW POWER(DT CRB0.7)

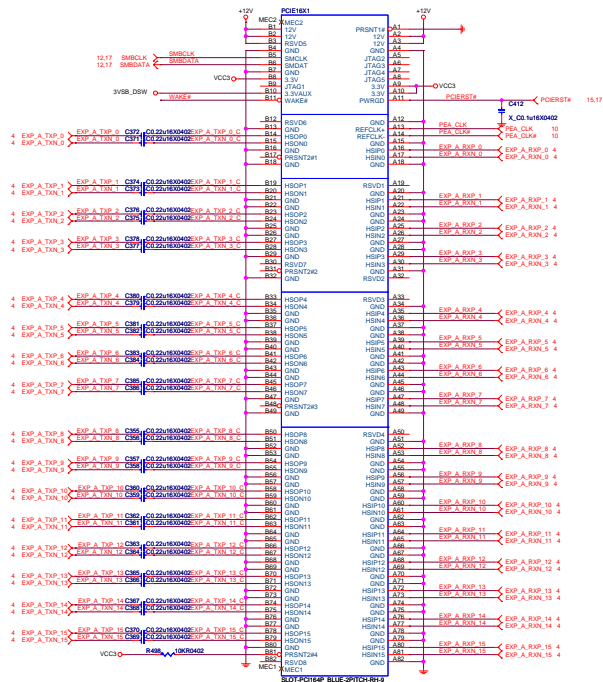


AGI Connect To VCC3 POWER(DT CRB0.7)

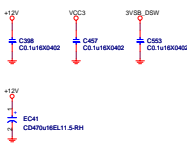


Place C283, C237 near P14, P16, P17, P26, P28
C285 near M14 C288 near U12 C289 near W14
C291 near AB2 C295 near V16 C297 near AA16, W16
C300 near AP22, AP19
Place C303 near AV4, AR4, AT5, AP5
C634 near AG1 C633 near W30 C304 near AP26
Place C630 near AM3 C301 near AK20
C631 near AW26 C302 near AP35
Place C635 near T14
Place C636 near AW39
Place C312, C311 near AD17, AD19
Place C306 near AW21 C632 near B6

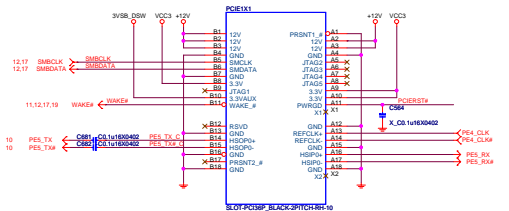
PCI EXPRESS X16 SLOT



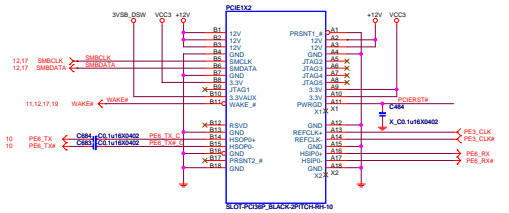
EXP_A_TXP_0



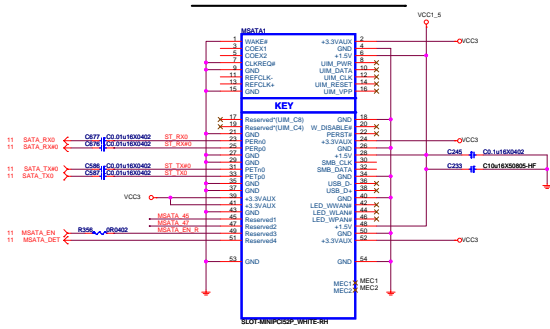
PCI EXPRESS x1 SLOT



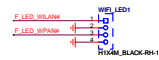
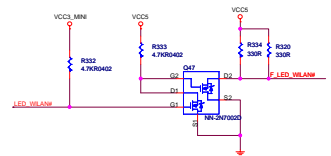
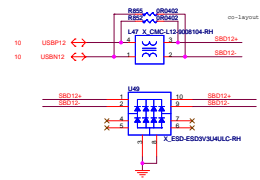
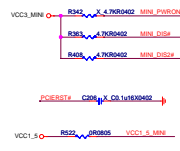
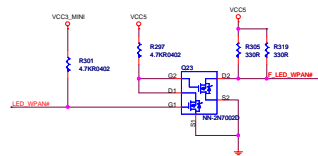
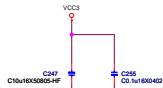
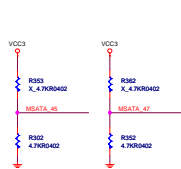
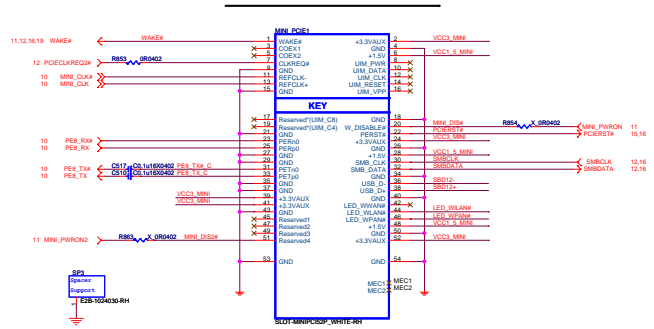
PCI EXPRESS x1 SLOT



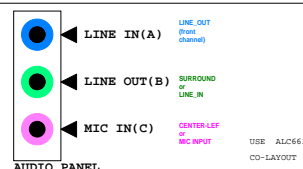
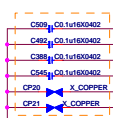
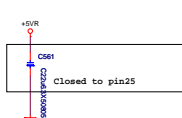
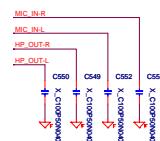
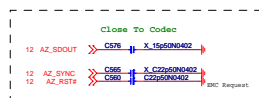
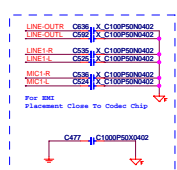
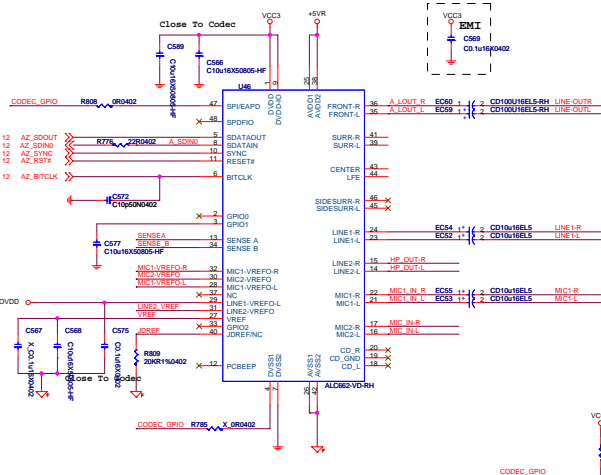
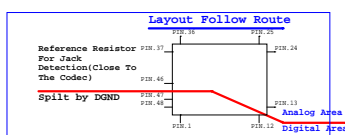
Full-size Mini SATA Card



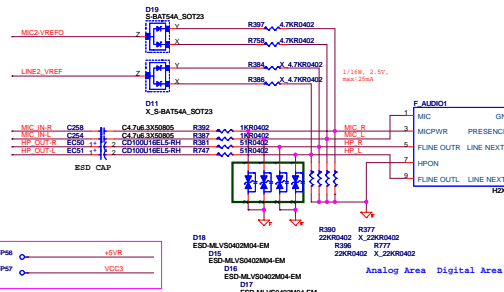
Half-size Mini PCIE Card



Azalia Codec -ALC662

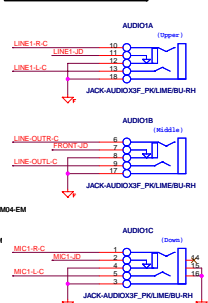


Front Audio Jack

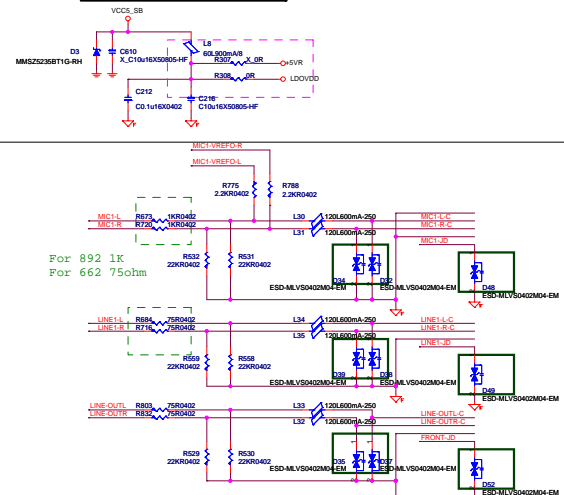


EMC Request

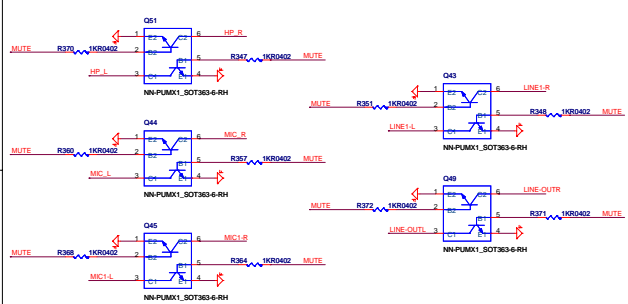
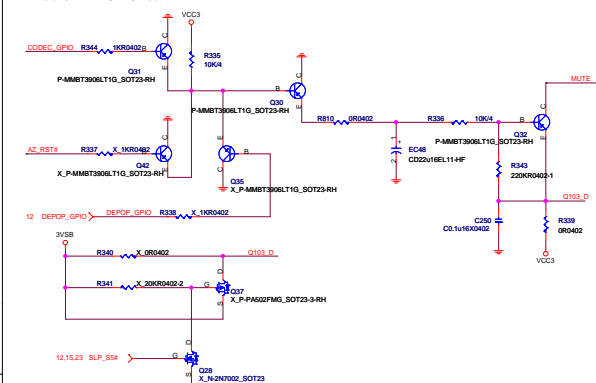
3 Jack Colay 6 Jack



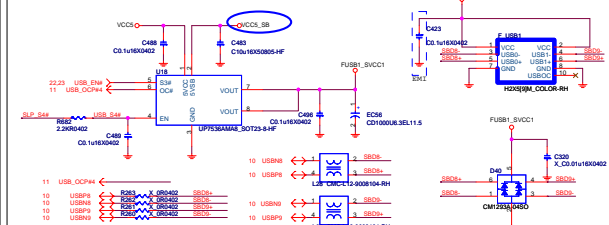
AUDIO CODE REGULATORS



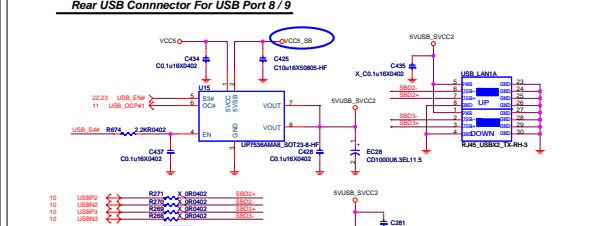
Audio DE-POP Circuit



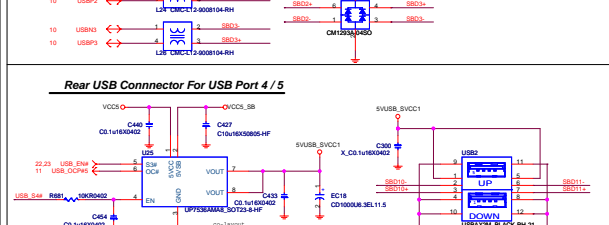
Front Panel USB Connector For USB Port 6 / 7



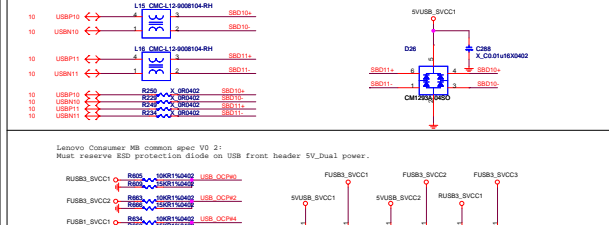
Rear USB Connector For USB Port 8 / 9



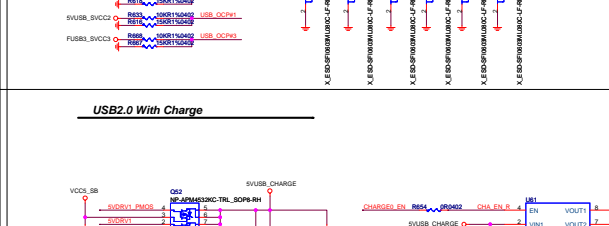
Rear USB Connector For USB Port 4 / 5



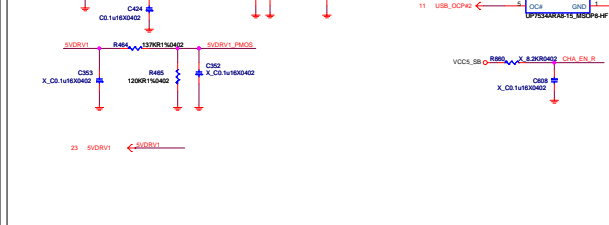
co-lay R3C-0000012-***



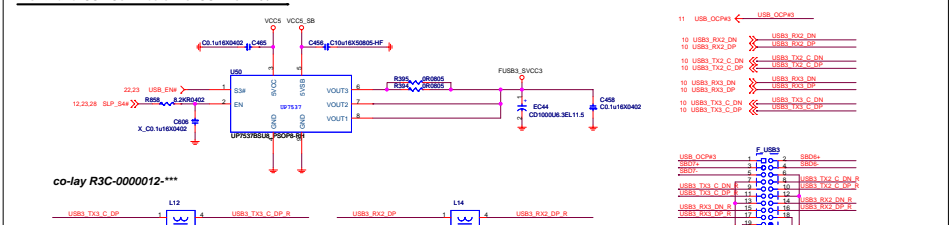
USB2.0 With Charge



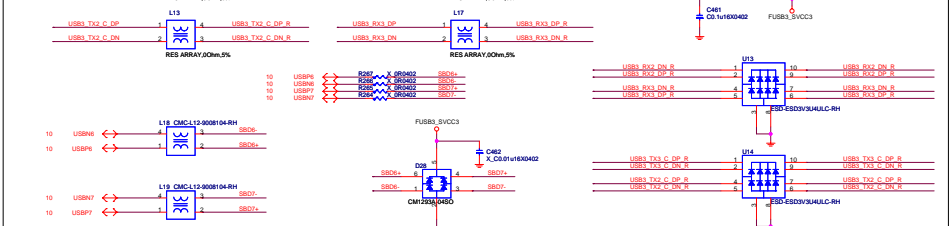
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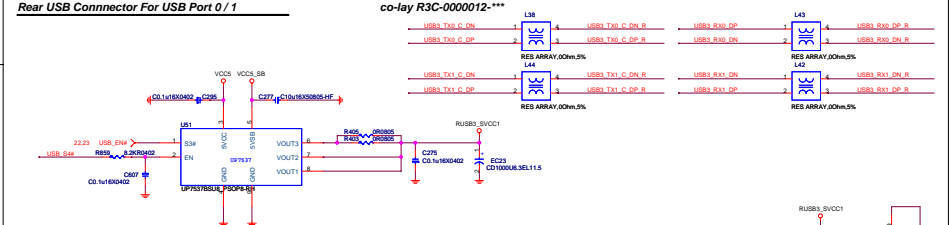
Front Panel USB Connector For USB Port 10 / 11



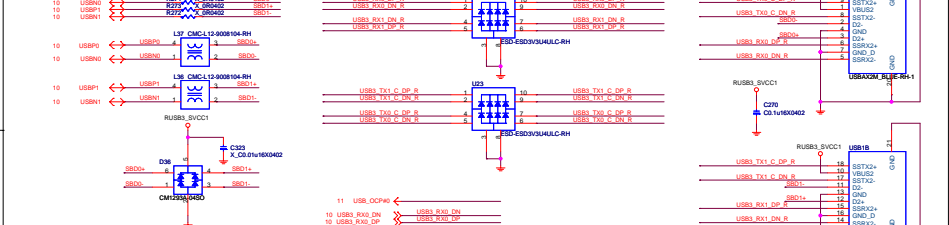
co-lay R3C-0000012-***



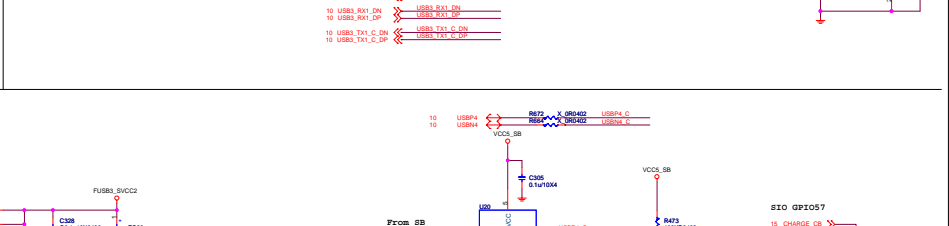
Rear USB Connector For USB Port 0 / 1



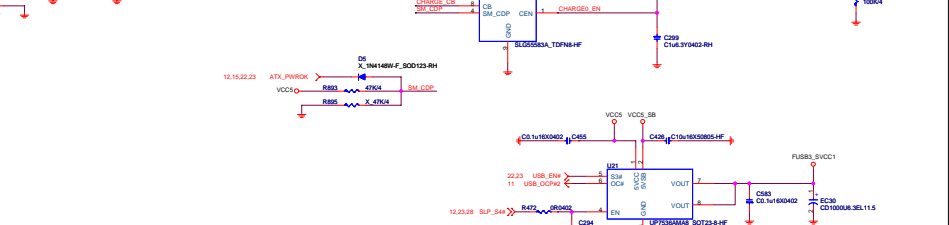
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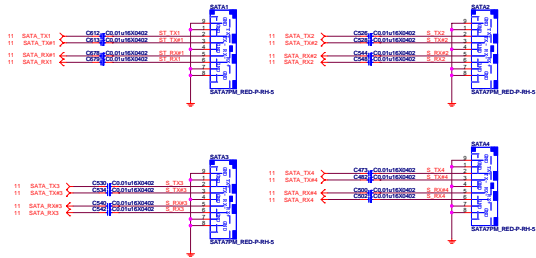
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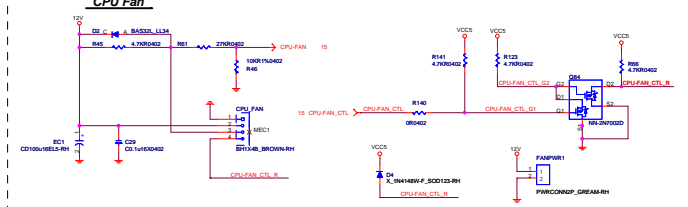
co-lay R3C-0000012-***



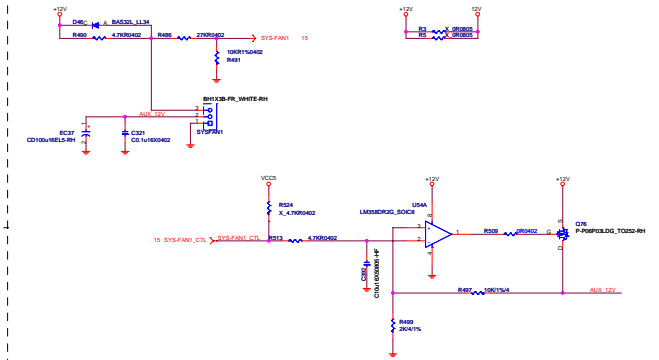
SATA Connector



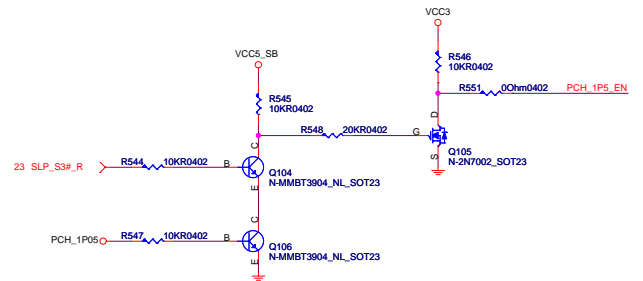
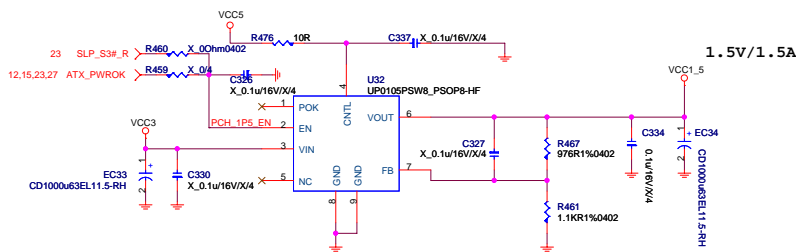
CPU Fan



System Fan

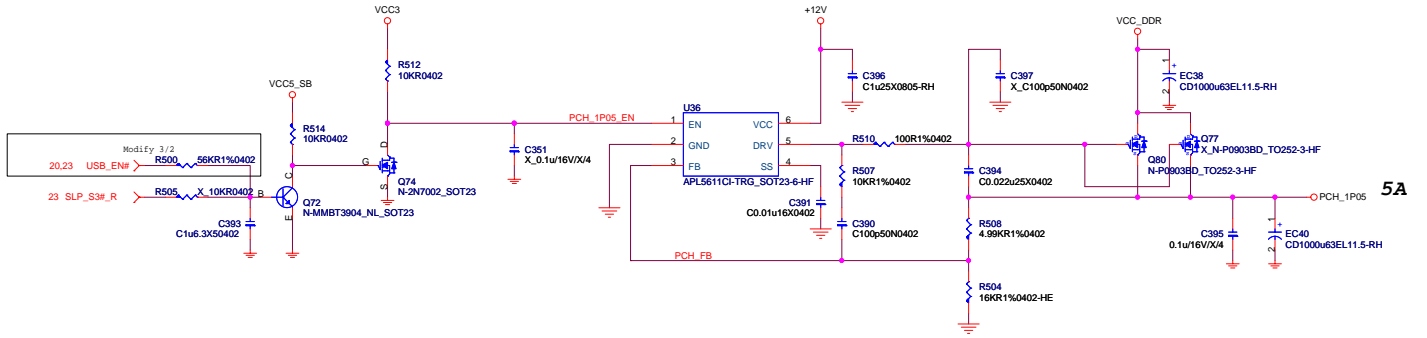


1.5V Power

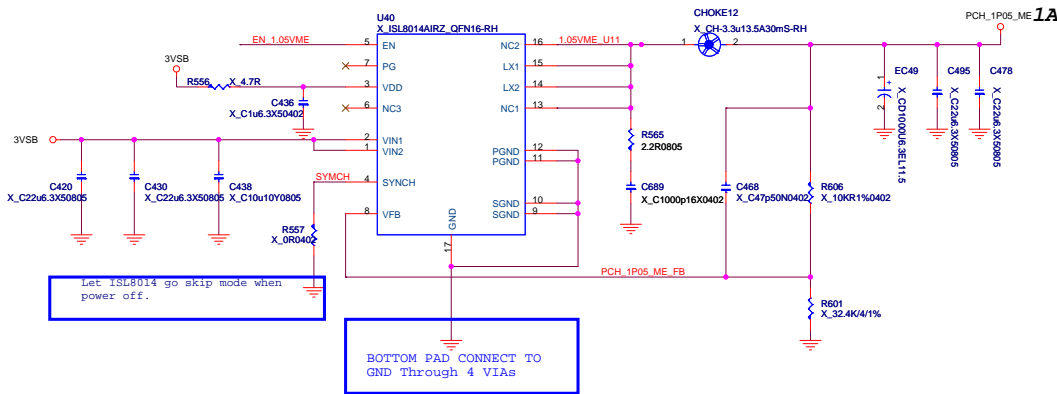


PCH Core Power Control

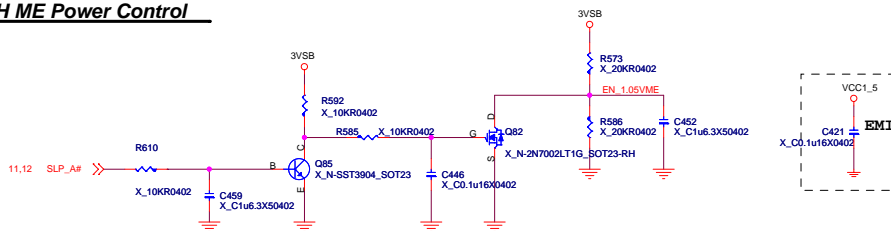
PCH Core Power



PCH ME Power

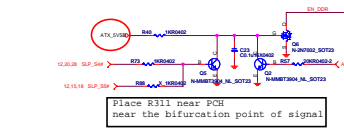
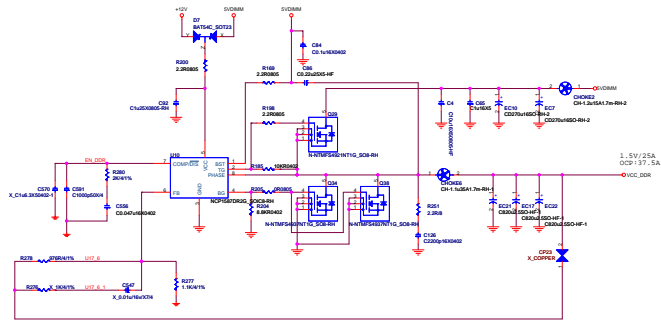


PCH ME Power Control



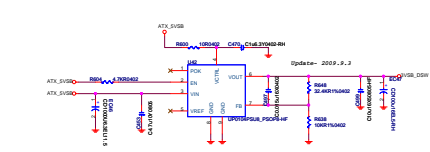
DDRIII DIMM Power

Vout = 0.81 (R254/R246) / R254



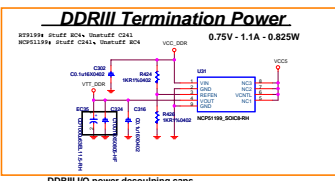
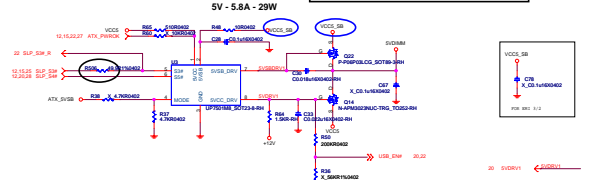
Deep Sx Power For Wake On Lan

Vout=0.8*(R461/R449)/(R461+3.392 V

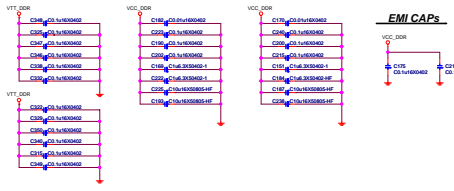


DDRIII Regulator Power Source

Place R86 near PCB, near the bifurcation point of signal



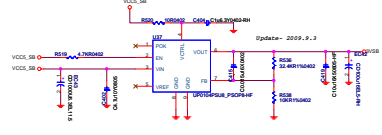
DDRIII IO power decoupling caps.



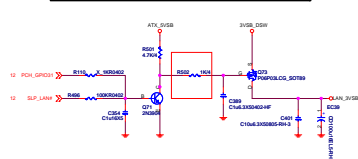
EMI CAPs



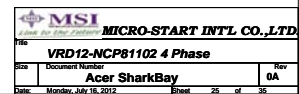
3V Standby Power

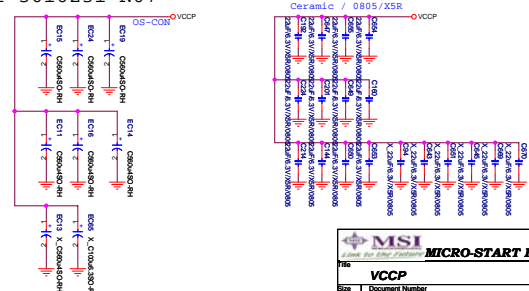
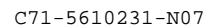
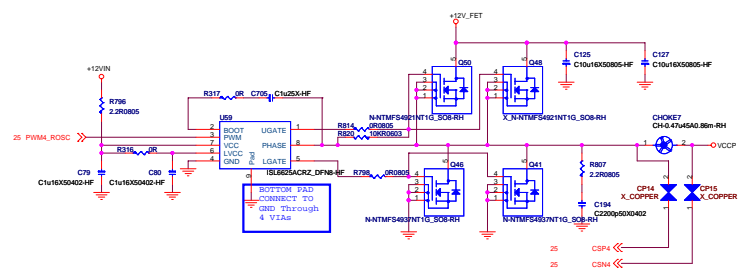
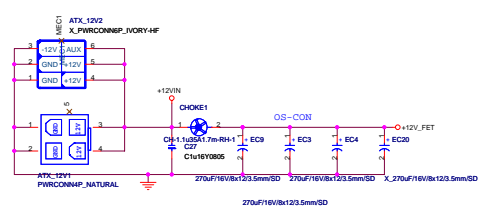


LAN Power

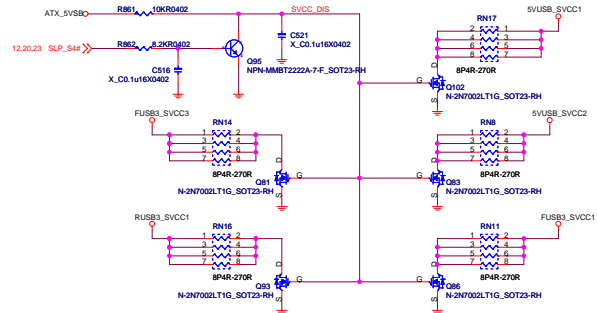
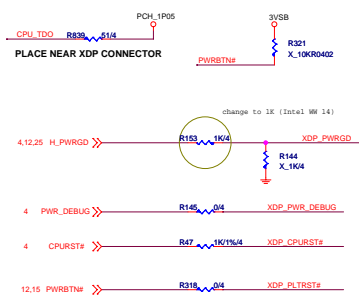


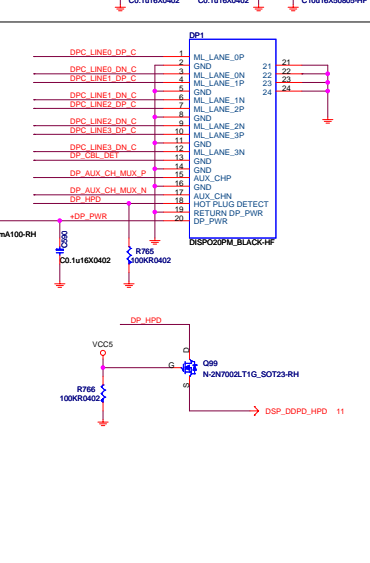
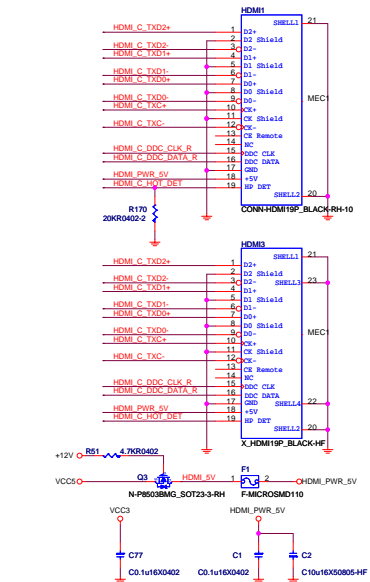
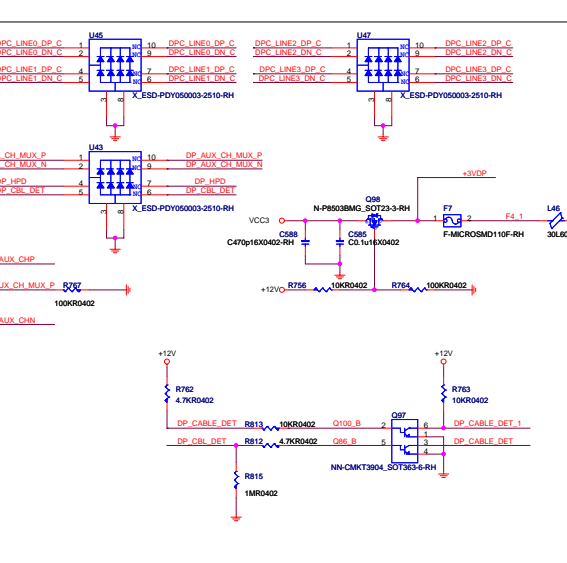
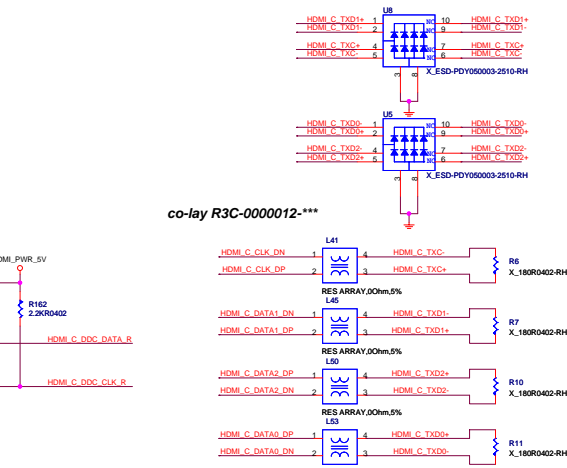
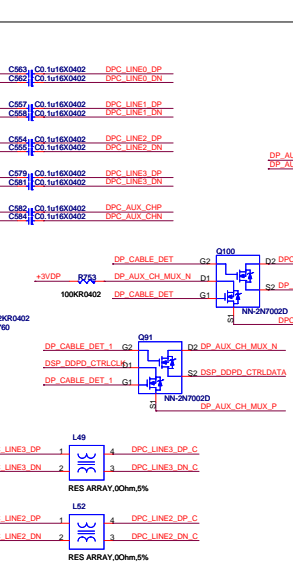
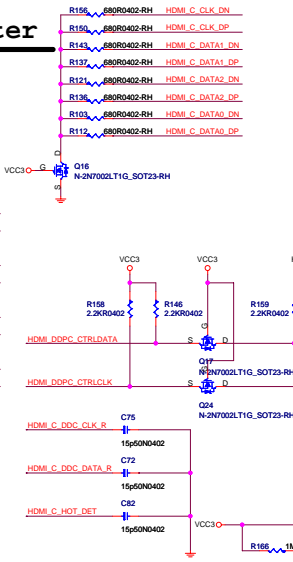
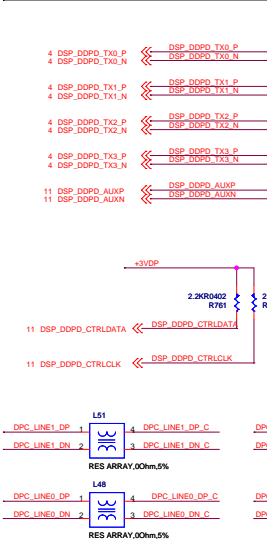
SharkBay VR12.5 Power Circuit - 4 Phase

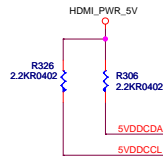
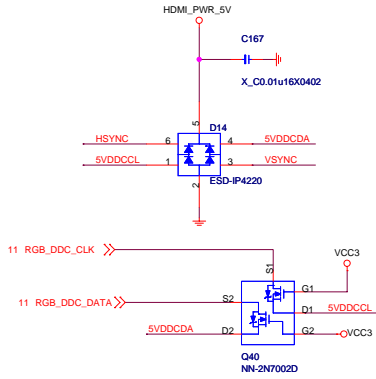
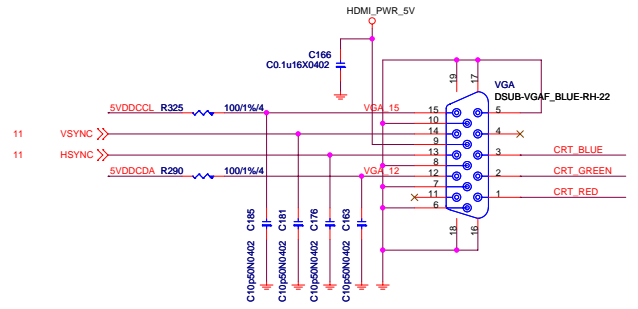
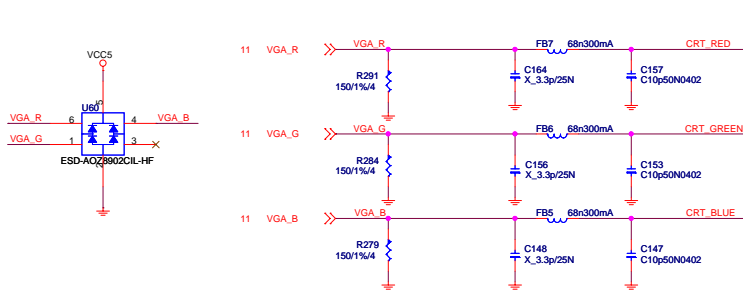




USB power discharge circuit



[illegible]



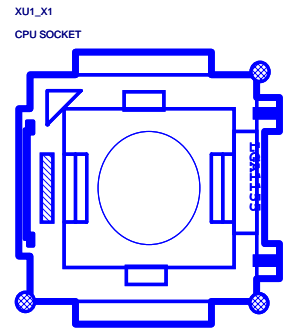
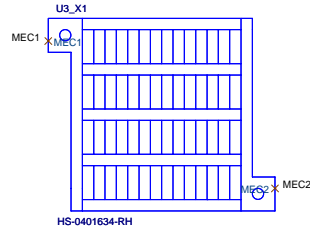
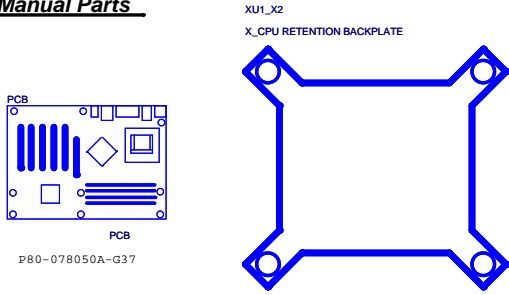
MSI
Micro Start Int'l Co., Ltd.
MICRO-START INT'L CO.,LTD

Title: **VGA**

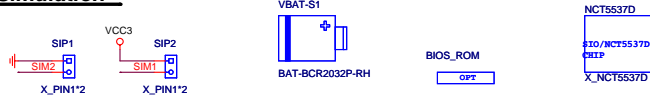
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Date: Friday, July 06, 2012 Sheet: 30 of 35

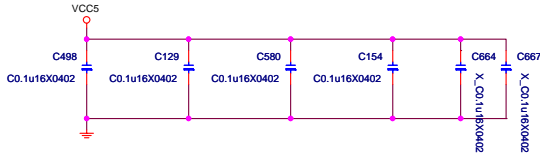
Manual Parts



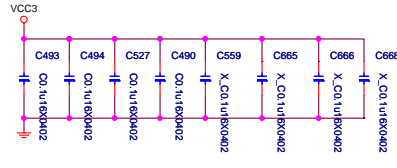
Simulation



For EMI

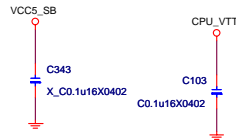


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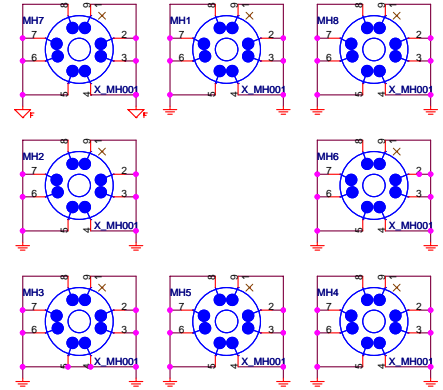


Optics Orientation Holes

Optical Fiducial Marks-120



Mounting Holes



MSI
Link to the Future

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Title

Manual & Option Parts

Size Document Number

Acer SharkBay

Date: Monday, July 16, 2012

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Rev 0A

Timing diagram for the SPI interface between the Board and the Slave. The diagram shows the relationship between the Board's CSn, SCLK, and SLP signals and the Slave's CSn, SCLK, and SLP signals. The Board's CSn signal is active-low and transitions from high to low at the start of the data transfer. The Board's SCLK signal is a continuous clock signal. The Board's SLP signal is active-low and transitions from high to low at the start of the data transfer. The Slave's CSn signal is active-low and transitions from high to low at the start of the data transfer. The Slave's SCLK signal is a continuous clock signal. The Slave's SLP signal is active-low and transitions from high to low at the start of the data transfer. The data transfer is shown as a series of bits being sent from the Board to the Slave. The Slave's CSn signal is active-low and transitions from high to low at the start of the data transfer. The Slave's SCLK signal is a continuous clock signal. The Slave's SLP signal is active-low and transitions from high to low at the start of the data transfer. The data transfer is shown as a series of bits being sent from the Board to the Slave.

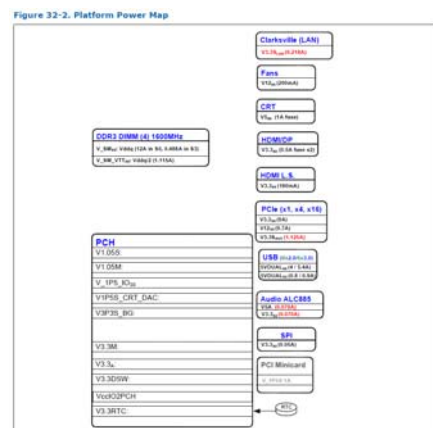
[illegible][illegible]

```

graph TD
    Processor[Intel 1150 Processor] -- CPU#0 --> PCH[PCH]
    ALC[ALC IP2 HD Codec] -- AL#0#2 --> PCH
    Reset[RESET SW] -- PP#0#2 --> PCH
    PCH -- P#0 --> SIO[Super I/O NCT5533D]
    SIO -- PCH#0 --> PCH
    SIO -- PCH#1 --> PCH
    SIO -- PCH#2 --> PCH
    SIO --> CPU_XDP[CPU XDP]
    SIO --> PCH_XDP[PCH XDP]
    SIO --> LAN[LAN 8111]
    SIO --> TPM[TPM]
    SIO --> AssetID[Asset ID]
    SIO --> PCH0[PCH#0 Slot]
    SIO --> PCH1[PCH#1 Slot]
    SIO --> MPCI[MPIC/MSATA Slot]
  
```

Diagram showing pins 1 through 16 of the ATmega328P microcontroller. The pins are labeled as follows:

- 12V
- 5V
- 3.3V
- 5VDRV1
- VCC1_5REF
- DDR_EN
- VCC1_5
- VCC_DDR
- PCH_1P05
- CHIP_PWRGD
- MEM_PWRGD
- H_PWRGD
- VCCCP
- PCH_SYSPWROK
- SUS_STAT#
- PLTRST#



PCH						
GPIO	All Function	VIOC	Power	Tel	Default	Signal Name
GPIO[0]	BMBUSIF#	IO	Main	3.3V	GPI	Puls-H
GPIO[1]	Unmused	IO	Main	3.3V	GPI	Puls-H
GPIO[2]	PIRQ0#	IO	Main	5V	GPI	SPL_WPR_PCH
GPIO[3]	PIRQF#	IO	Main	5V	GPI	Puls-H
GPIO[4]	PIRQ0#	IO	Main	5V	GPI	Puls-H
GPIO[5]	PIRQ#	IO	Main	5V	GPI	Puls-H
GPIO[6]	Unmused	IO	Main	3.3V	GPI	Puls-H
GPIO[7]	Unmused	IO	Main	3.3V	GPI	Puls-H
GPIO[8]	Unmused	IO	Resume	3.3V	GPO	Puls-H
GPIO[9]	OC5#	IO	Resume	3.3V	Native	USB_OC#0#
GPIO[10]	OC6#	IO	Resume	3.3V	Native	USB_OC#0#
GPIO[11]	SMBALERT#	IO	Resume	3.3V	Native	Puls-H
GPIO[12]	LAN_PHY_PWR_CTRL	IO	Resume	3.3V	Native	LAN_DISABLE#
GPIO[13]	Unmused	IO	Resume	3.3V	GPI	PCH_SMR#
GPIO[14]	OC7#	IO	Resume	3.3V	Native	SIO_PMR#
GPIO[15]	Unmused	IO	Resume	3.3V	GPO	Puls-H
GPIO[16]	SATAAGP	IO	Main	3.3V	GPI	Puls-Low
GPIO[17]	Unmused	IO	Main	3.3V	GPI	CLK_CMOS
GPIO[18]	PCICLKRQ1#	IO	Main	3.3V	Native	Puls-H
GPIO[19]	SATAAGP	IO	Main	3.3V	GPI	Puls-H
GPIO[20]	PCICLKRQ2#	IO	Main	3.3V	Native	PCICLKRQ2#
GPIO[21]	SATAAGP	IO	Main	3.3V	GPI	Puls-H
GPIO[22]	SCLK	IO	Main	3.3V	GPI	LPT_DET#
GPIO[23]	LDRQ1#	IO	Main	3.3V	Native	NC
GPIO[24]	Unmused	IO	Resume	3.3V	GPO	MRN_PWRON
GPIO[25]	Unmused	IO	Resume	3.3V	Native	Puls-H
GPIO[26]	Unmused	IO	Resume	3.3V	Native	Puls-H
GPIO[27]	Unmused	IO	DSW	3.3V	GPI	Puls-H
GPIO[28]	Unmused	IO	Resume	3.3V	GPO	Puls-H
GPIO[29]	SLP_WLAN#	IO	Resume	3.3V	Native	NC
GPIO[30]	SUS_PWRON_ACK/SUS_WARM#	IO	Resume	3.3V	GPI	PCH_SUSWRARM#
GPIO[31]	Unmused	IO	DSW	3.3V	GPI	Puls-H
GPIO[32]	Unmused	IO	Main	3.3V	GPO	CLKRUN#
GPIO[33]	HOA_DOCK_EN#	IO	Main	3.3V	GPO	Puls-H
GPIO[34]	STP_PC1	IO	Main	3.3V	GPI	Puls-H
GPIO[35]	Unmused	IO	Main	3.3V	GPO	Puls-H
GPIO[36]	SATAAGP	IO	Main	3.3V	GPI	NC

PIN NAME	USAGE	Input/Output	NOTES
GPIO0	AUX_FAN1_CTL	Output	Fan speed control
GPIO4	AUX_FAN1	Input	Fan speed sense
GPIO20	KBDATA	Input	Keyboard data in
GPIO21	KBCLK	Output	keyboard clock out
GPIO22	MSDATA	Input	Mouse data in
GPIO23	MSCLK	Output	Mouse clock out
GPIO34	SIO_WAKE#_R	Output	Wake up signal from LAN
GPIO25	AMPWVR_EN	Input	Pin strap which disabled AMP power sequence
GPIO28	SIO_GP2#	Output	Reserved GPIO for future use
GPIO41	SMR#	Output	SIO SMR generation
GPIO42	SDA_SIO	Output	Reserved GPIO for future use
GPIO54	SLP_SUS#	Input	DSW signal which received from PCH
GPIO56	PS2_DET#	Input	PS2 device detect signal
GPIO57	PWR_LED_R	Output	LED drive signal which shows the system state

PIN NAME	USAGE	Input/Output	NOTES
GPIO0	AUX_FAN1_CTL	Output	Fan speed control
GPIO1	NA	NA	NA
GPIO2	NA	NA	NA
GPIO3	NA	NA	NA
GPIO4	AUX_FAN1	Input	Fan speed sense
GPIO5	AUX_FAN2	Input	Pull low
GPIO6	AUX_FAN3	Input	Pull low
GPIO7	NA	NA	NA
GPIO10	RBB#	Input	Com port signal
GPIO11	OC0B#	Input	Com port signal
GPIO12	SOUTB#	Output	Com port signal
GPIO13	SINB	Input	Com port signal
GPIO14	OTR0B#	Output	Com port signal
GPIO15	RT0B#	Output	Com port signal
GPIO16	OT0B#	Input	Com port signal
GPIO17	CT0B#	Input	Com port signal
GPIO20	KBDATA	Input	Keyboard data in
GPIO21	KBCLK	Output	keyboard clock out
GPIO22	MSDATA	Input	Mouse data in
GPIO23	MSCLK	Output	Mouse clock out

PCH						
GPIO	All Function	VIOC	Power	Tel	Default	Signal Name
GPIO[37]	SATAAGP	IO	Main	3.3V	GPI	Puls-H
GPIO[38]	SLOAD	IO	Main	3.3V	GPI	CHASSIS_ID1
GPIO[39]	SDATAOUT0	IO	Main	3.3V	GPI	CHASSIS_ID2
GPIO[40]	OC1#	IO	Resume	3.3V	Native	USB_OC#1#
GPIO[41]	OC2#	IO	Resume	3.3V	Native	USB_OC#2#
GPIO[42]	OC3#	IO	Resume	3.3V	Native	USB_OC#3#
GPIO[43]	OC4#	IO	Resume	3.3V	Native	USB_OC#4#
GPIO[44]	PCICLKRQ0#	IO	Resume	3.3V	Native	PCICLKRQ0#
GPIO[45]	PCICLKRQ0#	IO	Resume	3.3V	Native	Puls-H
GPIO[46]	PCICLKRQ7#	IO	Resume	3.3V	Native	S.M. SEL
GPIO[48]	SDATAOUT1	IO	Main	3.3V	GPI	CORP_SPD1
GPIO[49]	SATAAGP	IO	Main	3.3V	GPI	MSATA_MPCIE_DET
GPIO[50]	Unmused	IO	Main	3.3V	GPI	FUSB_01
GPIO[51]	Unmused	IO	Main	3.3V	GPO	NC
GPIO[52]	Unmused	IO	Main	3.3V	GPI	FUSB_02
GPIO[53]	Unmused	IO	Main	3.3V	GPO	NC
GPIO[54]	Unmused	IO	Main	3.3V	GPI	Puls-H
GPIO[55]	Unmused	IO	Main	3.3V	GPO	NC
GPIO[56]	Unmused	IO	Resume	3.3V	GPI	Puls-H
GPIO[58]	SMLCLK#	IO	Resume	3.3V	Native	CTL1
GPIO[59]	OC5#	IO	Resume	3.3V	Native	USB_OC#5#
GPIO[60]	SMBALERT#	IO	Resume	3.3V	Native	Puls-H
GPIO[61]	SUS_STAT#	IO	Resume	3.3V	Native	SUS_STAT#
GPIO[62]	SUSCLK	IO	Resume	3.3V	Native	NC
GPIO[63]	SLP_SS#	IO	Resume	3.3V	Native	SLP_SS#
GPIO[64]	CLKOUTFLEX0	IO	CORE	3.3V	Native	NC
GPIO[65]	CLKOUTFLEX1	IO	CORE	3.3V	Native	NC
GPIO[66]	CLKOUTFLEX2	IO	CORE	3.3V	Native	NC
GPIO[67]	CLKOUTFLEX3	IO	CORE	3.3V	Native	CLKOUTFLEX3_40M
GPIO[68]	Unmused	IO	CORE	3.3V	GPI	Puls-H
GPIO[69]	Unmused	IO	CORE	3.3V	GPI	Puls-H
GPIO[70]	Unmused	IO	CORE	3.3V	GPI	MSATA_EN
GPIO[71]	Unmused	IO	CORE	3.3V	GPI	Puls-H
GPIO[72]	Unmused	IO	DSW	3.3V	Native	Puls-H
GPIO[73]	PCICLKRQ0#	IO	Resume	3.3V	Native	CTL3
GPIO[74]	SMBALERT#	IO	Resume	3.3V	Native	Puls-H
GPIO[75]	SMLIDATA	IO	Resume	3.3V	Native	CTL2

PIN NAME	USAGE	Input/Output	NOTES
GPIO80	CTSA#	Input	LPT signal
GPIO81	DSRA#	Input	LPT signal
GPIO82	RTSA#	Output	LPT signal
GPIO83	OTRA#	Output	LPT signal
GPIO84	SINA	Input	LPT signal
GPIO85	SOUTA	Output	LPT signal
GPIO86	DCDA#	Input	LPT signal
GPIO87	RIAA	Input	LPT signal

DDR-III DIMM Config		
DEVICE	ADDRESS(SA1:SA0)	CLOCK
DIMM 1	01	MEM_MA_CLK_H2L2 MEM_MA_CLK_H3L3
DIMM2	00	MEM_MA_CLK_H0L0 MEM_MA_CLK_H1L1
DIMM 3	11	MEM_MB_CLK_H0L2 MEM_MB_CLK_H3L3
DIMM 4	10	MEM_MB_CLK_H0L0 MEM_MB_CLK_H1L1

PIN NAME	USAGE	Input/Output	NOTES
GPIO24	SIO_WAKE#_R	Output	Wake up signal from LAN
GPIO25	AMPWVR_EN	Input	Pin strap which disabled AMP power sequence
GPIO28	NA	NA	NA
GPIO27	MLE0	Output	Pull high
GPIO30	RESETCON#	Input	Pull high
GPIO31	SDA_SIO	Output	Reserved GPIO for future use
GPIO32	SCL_SIO	Output	Reserved GPIO for future use
GPIO33	NA	NA	NA
GPIO34	PRSTB#	Output	LPT signal
GPIO35	PRAFD#	Output	LPT signal
GPIO36	PRERR#	Input	LPT signal
GPIO40	TEST_MODE_EN	Input	Pin strap which disabled test mode
GPIO41	PRINT#	Output	LPT signal
GPIO42	LPT_SLN#	Output	LPT signal
GPIO43	PRACK#	Input	LPT signal
GPIO44	PRBUSY	Input	LPT signal
GPIO45	PRPE	Input	LPT signal
GPIO46	PRSLCT	Input	LPT signal
GPIO47	RESETCON#	Input	Pull high
GPIO50	SUSWRARM#	Output	DSW signal

PIN NAME	USAGE	Input/Output	NOTES
GPIO51	SIO_EVDUAL	Input	DSW signal
GPIO52	SUBACK#	Output	DSW signal
GPIO53	NA	NA	NA
GPIO54	SLP_SUS#	Input	DSW signal
GPIO55	SVSSVSB_OFF_R	Output	DSW signal
GPIO56	PS2_DET#	Input	PS2 detect signal
GPIO57	PWR_LED_R	Output	Power led
GPIO60	RND0	IO	LPT signal
GPIO61	RND1	IO	LPT signal
GPIO62	RND2	IO	LPT signal
GPIO63	RND3	IO	LPT signal
GPIO64	RND4	IO	LPT signal
GPIO65	RND5	IO	LPT signal
GPIO66	RND6	IO	LPT signal
GPIO67	RND7	IO	LPT signal
GPIO70	DSW_EN	Input	Pin strap which enable DSW
GPIO71	SIO_GP71	Output	Reserved GPIO for future use
GPIO72	SIO_GP72	Output	Reserved GPIO for future use
GPIO73	SIO_GP73	Output	Reserved GPIO for future use
GPIO74	RSTOUT0#	Output	PCIe reset signal

PIN NAME	USAGE	Input/Output	NOTES
GPIO75	RSTOUT1#	Output	LPC_Debbug card reset signal
GPIO76	RSTOUT2#	Output	TPM reset signal
GPIO80	CTSA#	Input	COM port signal
GPIO81	DSRA#	Input	COM port signal
GPIO82	RTSA#	Output	COM port signal
GPIO83	OTRA#	Output	COM port signal
GPIO84	SINA	Input	COM port signal
GPIO85	SOUTA	Output	COM port signal
GPIO86	DCDA#	Input	COM port signal
GPIO87	RIAA	Input	COM port signal

